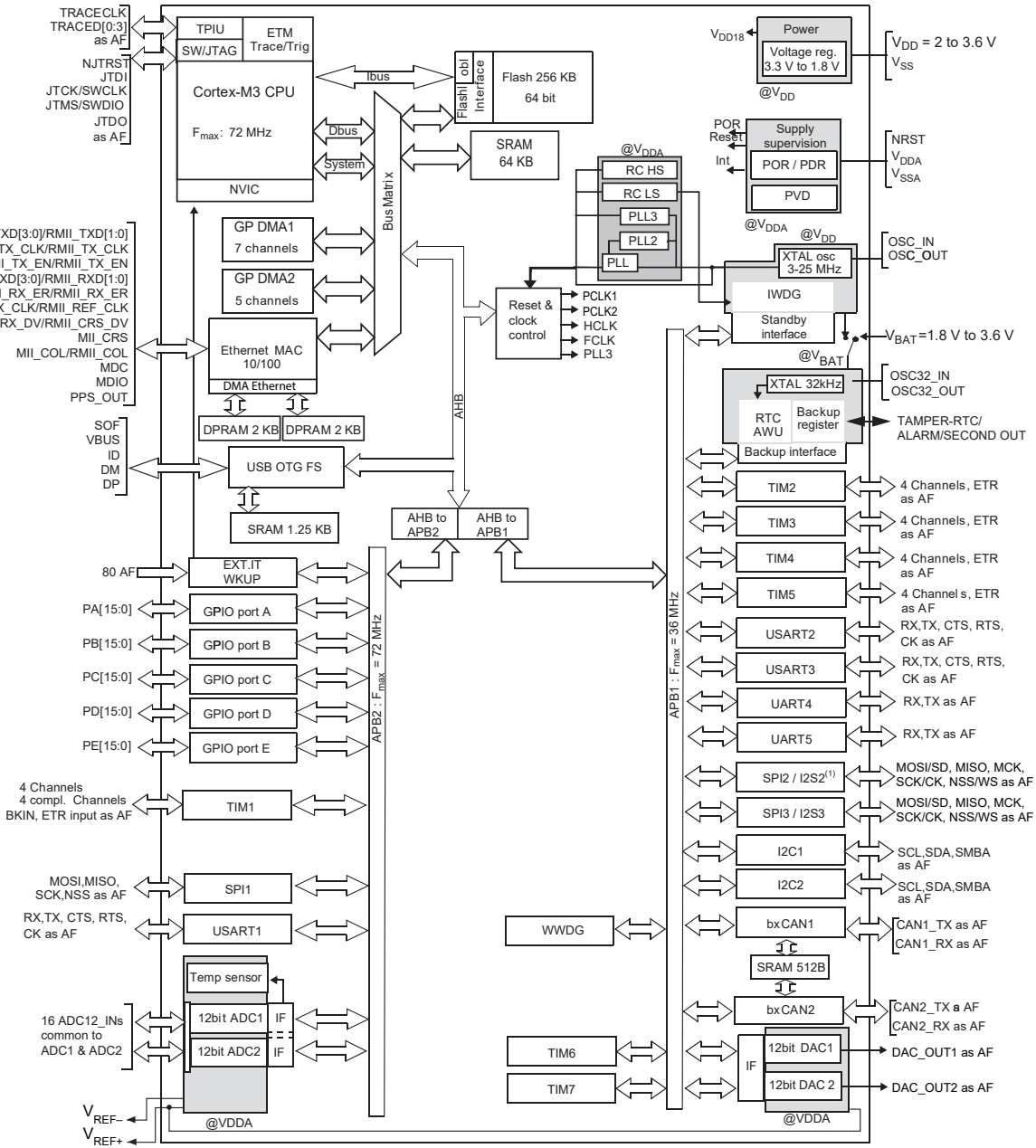
TRACECLK
TRACED[0:3]
as AF
NJTRST
JTDI
JTCK/SWCLK
JTMS/SWDIO
JTDO
as AF
TPIU
ETM
Trace/Trig
SW/JTAG
Cortex-M3 CPU
Fmax: 72 MHz
NVIC
Ibus
Dbus
System
Bus Matrix
Flash Interface
Flash 256 KB
64 bit
SRAM
64 KB
VDD18
Power
Voltage reg.
3.3 V to 1.8 V
@VDD
VDD = 2 to 3.6 V
VSS
POR
Reset
Int
Supply
supervision
POR / PDR
PVD
@VDDA
NRST
VDDA
VSSA
@VDDA
RC HS
RC LS
PLL3
PLL2
PLL
@VDD
XTAL osc
3-25 MHz
OSC_IN
OSC_OUT
MII_TXD[3:0]/RMII_TXD[1:0]
MII_TX_CLK/RMII_TX_CLK
MII_TX_EN/RMII_TX_EN
MII_RXD[3:0]/RMII_RXD[1:0]
MII_RX_ER/RMII_RX_ER
MII_RX_CLK/RMII_REF_CLK
MII_RX_DV/RMII_CRS_DV
MII_CRS
MII_COL/RMII_COL
MDC
MDIO
PPS_OUT
GP DMA1
7 channels
GP DMA2
5 channels
Ethernet MAC
10/100
DMA Ethernet
Reset &
clock
control
PCLK1
PCLK2
HCLK
FCLK
PLL3
IWDG
Standby
interface
VBAT=1.8 V to 3.6 V
@VBAT
XTAL 32kHz
RTC
AWU
Backup
register
Backup interface
OSC32_IN
OSC32_OUT
TAMPER-RTC/
ALARM/SECOND OUT
SOF
VBUS
ID
DM
DP
DPRAM 2 KB
DPRAM 2 KB
USB OTG FS
SRAM 1.25 KB
AHB
AHB to
APB2
AHB to
APB1
80 AF
EXT.IT
WKUP
PA[15:0]
GPIO port A
PB[15:0]
GPIO port B
PC[15:0]
GPIO port C
PD[15:0]
GPIO port D
PE[15:0]
GPIO port E
APB2 : Fmax = 72 MHz
APB1 : Fmax = 36 MHz
TIM2
4 Channels, ETR
as AF
TIM3
4 Channels, ETR
as AF
TIM4
4 Channels, ETR
as AF
TIM5
4 Channels, ETR
as AF
USART2
RX,TX, CTS, RTS,
CK as AF
USART3
RX,TX, CTS, RTS,
CK as AF
UART4
RX,TX as AF
UART5
RX,TX as AF
SPI2 / I2S2(1)
MOSI/SD, MISO, MCK,
SCK/CK, NSS/WS as AF
SPI3 / I2S3
MOSI/SD, MISO, MCK,
SCK/CK, NSS/WS as AF
I2C1
SCL,SDA,SMBA
as AF
I2C2
SCL,SDA,SMBA
as AF
bxCAN1
CAN1_TX as AF
CAN1_RX as AF
SRAM 512B
bxCAN2
CAN2_TX as AF
CAN2_RX as AF
4 Channels
4 compl. Channels
BKIN, ETR input as AF
TIM1
MOSI,MISO,
SCK,NSS as AF
SPI1
RX,TX, CTS, RTS,
CK as AF
USART1
WWDG
Temp sensor
16 ADC12_INs
common to
ADC1 & ADC2
12bit ADC1
12bit ADC2
IF
IF
TIM6
TIM7
IF
12bit DAC1
12bit DAC 2
DAC_OUT1 as AF
DAC_OUT2 as AF
VREF–
VREF+
@VDDA
@VDDA

ai15411